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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,462	05/11/2005	Daniel Chatroux	123886	5027

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EXAMINER	
MEMULA, SURESH	
ART UNIT	**PAPER NUMBER**
2825	

NOTIFICATION DATE	DELIVERY MODE
02/04/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/534,462	CHATROUX ET AL.	
	Examiner	Art Unit	
	SURESH MEMULA	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-31 and 33-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-31 and 33-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is a response to the RCE filed on 12/08/2009. Pursuant to Applicant's amendments and remarks contained therein, the §102(e) rejections under Huang are withdrawn. However, in view of the newly considered combination of references detailed below, this application is not in condition for allowance. Claims 17-31 and 33-37 are pending, of which claim 32 is newly cancelled and claim 37 is newly added.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/08/2009 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claim 17-29, 31, 33-34, and 36-37 rejected under 35 U.S.C. 103(a)** as being unpatentable over US Patent 5,703,790 to Farwell (Hereinafter: Farwell) in view of US Pub. No. 2003/0155963 to Huang (Hereinafter: Huang).

4. **NOTE**: The Farwell reference is cited by Applicant in the PTO-1449 filed 05/11/2005 and the Huang reference was relied upon under §102(e) in the last office action.

5. As to claim 17 and similarly recited claim 36, **Farwell teaches**:

a power supply (Fig. 1: element 101 or 103);

a clock circuit emitting a clock signal (Col. 2, lines 37-41; Fig. 1: element 33);

a digital part comprising a plurality of subassemblies (Fig. 1: elements 11 and 21) each comprising:

a first power supply terminal (Fig. 1: elements 13 and 23);

a second power supply terminal (Fig. 1: elements 15 and 25);

a processor connected between the first and second power supply terminals (Fig. 1: elements 11 and 21);

the subassemblies are connected in series by means of their first and second power supply terminals between terminals of a voltage supply source (Col. 1, lines 33-36; Fig. 1: subassemblies 11 and 21 are connected in series between voltage supply source 101 and 103); and

wherein the second subassembly includes a clock input coupled to the clock circuit (Col. 2, lines 37-41; Fig. 1: subassembly 21 includes a clock input for receiving a clock signal from clock circuit 33); and

a level shifter connected between the clock circuit and the clock input of at least one of the subassemblies (Col. 2, lines 37-41; i.e., a VCO provides a variable clock signal to the second subassembly), wherein the level shifter is configured to adapt the clock signal to a voltage between the first and second power supply terminals of the at least one of the subassemblies (Col. 2, lines 29-41; i.e., the VCO outputs a variable clock signal in a proportional manner relative to voltage difference at the power supply terminal).

.

6. As detailed above, Farwell discloses the second subassembly includes a clock input from the clock circuit but does not explicitly detail the first subassembly includes a clock input from the clock circuit. Therefore, **Farwell does not explicitly teach** each subassembly includes a clock input coupled to the clock circuit.

7. **Huang teaches** each subassembly (Fig. 2: e.g., Subassembly 1: elements 218-219 and Subassembly 2: elements 220-221) includes a clock input (Fig. 1: input line elements 210/211 and 212/213 corresponding to subassemblies 1 and 2) coupled to a clock circuit (Fig. 2: element CLK).

8. **It would have been obvious** to one of ordinary skill in the art to have combined the teachings of Farwell with Huang so as to detail each subassembly includes a clock input because such a connection allows for controlling the voltage of each subassembly (Huang: ¶22, 30) and additionally allows for controlling the processing rate of each subassembly (Farwell: Col. 2, lines 29-41).

9. As to claim 18, wherein the clock inputs of at least two adjacent subassemblies are connected by the level shifter (Farwell: Col. 2, lines 37-41; Huang: Fig. 2: elements 214-217 or 223-226).

10. As to claim 19, wherein the clock input of an end subassembly is connected by an additional level shifter at the output of the clock circuit (Huang: Fig. 2: Subassembly 218-219 with corresponding elements 222, 214-215, 223-224; or Subassembly 220-221 with corresponding elements 216-217, 225-226).

11. As to claim 20, wherein the level shifter comprises at least one capacitor (Huang: Fig. 2: elements 214-217).

12. As to claim 21, wherein the level shifter comprises at least one transistor (Huang: ¶21; Fig. 2: elements 223-226 or 218-222).

13. As to claim 22, wherein all the subassemblies are identical (Farwell: Fig. 1: elements 11 and 21 are both digital processors; Huang: Fig. 2: subassemblies 218-219 and 220-221 are both electrical components).

14. As to claim 23, wherein each of the subassemblies further comprises a voltage limiting circuit connected between the first and the second power supply terminals (Farwell: Fig. 1: elements 33, 37; Huang: ¶3, 19, 30-33; Fig. 2: elements 218-222).

15. As to claim 24, wherein the voltage limiting circuit comprises a diode (Huang: ¶3, 19, 30-33).

16. As to claim 25, wherein the voltage limiting circuit comprises a transistor (Huang: Fig. 2: elements 218-222).

17. As to claim 26, wherein each subassembly further comprises a decoupling capacitor connected between the first and second power supply terminals (Huang: Fig. 2: elements 214-217, C_{out}).

18. As to claim 27, wherein the integrated circuit further comprises electrical insulation between the subassemblies (Huang: ¶3, 19, 30-33; Fig. 2: elements 218-222).

19. As to claim 28, wherein the means for electrical insulation between the subassemblies are reverse biased diode junctions (Huang: ¶3-5, 19, 30-33; Fig. 1-2: elements 218-222).

20. As to claim 29, wherein the means for electrical insulation between the different subassemblies are dielectric zones (Huang: ¶3-5, 19, 30-33; Fig. 1-2: elements 218-222).

21. As to claim 31, wherein the subassemblies are at different electrical potentials (Farwell: Fig. 1: elements 101, 103; Huang: Fig. 2: Subassembly 218-219 is closer to a positive potential; Subassembly 220-221 is closer to a negative potential), and a potential difference between two end subassemblies is greater than a potential difference between terminals of each subassembly (Farwell: Fig. 1: elements 101, 103; Huang: Fig. 2, in example, at the Vdd end of subassembly 218-219 the potential is positive x, at the GND end of subassembly 220-221 the potential is zero; thus the difference of the ends is always x, and due to impedance is always greater than the individual potential at each subassembly.).

22. As to claim 33, wherein a same current flowing through different subassemblies varies by less than 20% (Farwell: Fig. 1: elements 11 and 21; Huang: Fig. 2: subassemblies 218-219 and 220-221; both Farwell and Huang's subassemblies are connected in series, thus the current, at all times, is equivalent and therefore less than 20%).

23. As to claim 34, wherein the subassemblies are formed in such a way that, at all times in operation, a same current flows through each of the subassemblies (Farwell:

Fig. 1: elements 11 and 21; Huang: Fig. 2: subassemblies 218-219 and 220-221; both Farwell and Huang's subassemblies are connected in series, thus the current, at all times, is the same).

24. As to claim 37, wherein an electrical current flows from a positive terminal of the power supply source to a negative terminal of the power supply source (Farwell: Fig. 1: elements 11, 21, 101, 103; i.e., Farwell's subassemblies are connected in series and between power supplies to form a closed circuit, thus the current flows from the positive terminal of a power supply source 101 to a negative terminal of a power supply source 103).

25. **Claim 35 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Farwell in view of Huang.

26. As to claim 35, **Farwell teaches**:

a clock circuit emitting a clock signal (Col. 2, lines 37-41; Fig. 1: element 33);

a digital part comprising a plurality of subassemblies (Fig. 1: elements 11 and 21) each comprising:

a first power supply terminal (Fig. 1: elements 13 and 23);

a second power supply terminal (Fig. 1: elements 15 and 25);

a processor connected between the first and second power supply terminals (Fig. 1: elements 11 and 21);

the subassemblies are connected in series by means of their first and second power supply terminals between terminals of a voltage supply source (Col. 1, lines 33-36; Fig. 1: subassemblies 11 and 21 are connected in series between voltage supply source 101 and 103); and

wherein the second subassembly includes a clock input coupled to the clock circuit (Col. 2, lines 37-41; Fig. 1: subassembly 21 includes a clock input for receiving a clock signal from clock circuit 33); and

a level shifter connected between the clock circuit and the clock input of at least one of the subassemblies (Col. 2, lines 37-41; i.e., a VCO provides a variable clock

signal to the second subassembly), wherein the level shifter is configured to adapt the clock signal to a voltage between the first and second power supply terminals of the at least one of the subassemblies (Col. 2, lines 29-41; i.e., the VCO outputs a variable clock signal in a proportional manner relative to voltage difference at the power supply terminal).

27. As detailed above, Farwell discloses the second subassembly includes a clock input for receiving a clock signal from the a level shifter of the clock circuit, but does not detail the first subassembly includes a clock input for receiving a clock signal from the clock circuit, wherein a same clock signal is applied to the second subassembly and to the first subassembly. Therefore, **Farwell does not teach** each subassembly comprises a clock input, wherein a same clock signal is applied to the clock input of all subassemblies.

28. **Huang teaches** subassemblies (Fig. 2: Subassembly 1: elements 218-219, Subassembly 2: elements 220-221), each comprising a clock input (Fig. 2: input line elements 210/211 and 212/213 corresponding to transistors 218-221), wherein a same/identical clock signal is applied to the clock input of all subassemblies (Fig. 2: element CLK at input of element 223).

29. **It would have been obvious** to one of ordinary skill in the art at the time of Applicant's invention to have combined the teachings of Farwell with Huang so as to detail each subassembly includes a clock input for receiving a clock signal that is the same for all subassemblies because, as realized by Huang, providing the level shifter devices to shift the levels of clock signals (Farwell: Col. 2, lines 37-41; Huang: Fig. 2: elements 214-217 or 222-226) allows for voltage amplification or reduction which in a multiple subassembly/stage circuit advantageously provides for selective voltage control (Farwell: Col. 2, lines 29-41; Huang: ¶13) and an overall stable output voltage (Farwell: Col. 1, lines 40-43; Huang: ¶11-12).

30. **Claim 30 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Farwell in view of Huang **in further view of one or more of**:

US Pub. No. 2004/0077151 to Bhattacharyya (Hereinafter: Bhattacharyya),

US Pub. No. 2004/0087084 to Hsieh (Hereinafter: Hsieh),

US Pub. No. 2004/0094763 to Agnello et al. (Hereinafter: Agnello), **or**

US Pub. No. 2004/0018668 to Maszara (Hereinafter: Maszara).

31. As to claim 30, **Farwell in view of Huang teaches** substantially all of the limitations of claim 17 from which claim 30 depends, but **Farwell in view of Huang does not explicitly teach** the IC comprising silicon-on-insulator.

32. **Bhattacharyya discloses** an IC comprising silicon-on-insulator (Abstract; ¶4, 15), **Hsieh discloses** an IC comprising silicon-on-insulator (¶24), **Agnello discloses** an IC comprising silicon-on-insulator (¶49), and **Maszara discloses** an IC comprising silicon-on-insulator (¶2).

33. **It would have been obvious** to one of ordinary skill in the art at the time of the Applicant's invention to have combined the teachings of Huang with one or more of Bhattacharyya, Hsieh, Agnello, or Maszara to utilize an IC comprising silicon-on-insulator in order to one or more of:

a. provide advantages of significant speed, power, and radiation immunity (Bhattacharyya: ¶4);
b. reduce undesired capacitance (Maszara: ¶2),
c. suppress short channel effect (Maszara: ¶2),
d. reduce latch-up and soft errors (Maszara: ¶2), **or**
e. implement well-documented (Maszara: ¶2), well-known (Hsieh: ¶ 24), and conventionally utilized (Bhattacharyya: Abstract; ¶15; Agnello: ¶49) SOI technology.

Response to Arguments

34. Applicant states:

(a) "Independent claims 1, 7, 35, and 36 are amended to clarify the recited structure, and to add a process connected between the first and second power supplies (Remarks: Page 7, ¶5)"; and

(b) "Huang's disclosure of a charge pump circuit, which is generally a higher output voltage when inputting a voltage regularly and comprising a boosting stage and at least one voltage multiplier cannot be reasonably be considered to teach any feature that corresponds to the digital part comprising the plurality of subassemblies; and a subassemblies comprising a processor, as is now recited, among other features, in each of the independent claims (Remarks: Page 8, ¶2)."

Examiner's response

35. **Regarding (a)**: Applicant's amendments to claims 7, 35, and 36 are sufficient to overcome the 102(e) rejections under Huang (Note: claim 1 is not a pending claim).

36. **Regarding (b)**: As disclosed in the above rejection, the teachings of Farwell are cited against Applicant's "digital part" and Applicant's remarks directed Huang are moot in view of the new grounds of rejection. However, as Applicant implies in remark (b) above, Huang remains wholly relevant to both Farwell teachings and Applicant's claims limitations directed to clock features.

37. Applicant's statement of Huang's disclosure of a charge pump circuit generally relating to a higher output voltage when inputting a voltage regularly (Remarks: Page 8, ¶2) is incomplete as a basis for disqualifying Huang as a reference under §103, because the statement fails to take into account the steps and elements involved in producing such an outcome. Specifically, Huang utilizes a level shifter (Huang: Fig. 2: elements 214-217 or 222-226) to shift the levels of a clock signal (Huang: Fig. 2: element "CLK"). Huang, and for this matter Farwell, disclose altering the clock signal allows for controlling of voltage (Huang: ¶22, 31; Farwell: Col. 2, lines 29-41).

Therefore, the portions of Huang cited in the above rejections remain pertinent to the issue of patentability regarding Applicant's pending claims, and reliance on the Huang reference is maintained.

Conclusion

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Suresh Memula whose telephone number is (571) 272-8046, and any inquiry for a formal Applicant initiated interview must be requested via a PTOL-413A form and faxed to the Examiner's personal fax phone number: (571) 273-8046. Furthermore, Applicant is invited to contact the Examiner via email (suresh.memula@uspto.gov) on the condition the communication is pursuant to and in accordance with MPEP §502.03 and §713.01. The Examiner can normally be reached Monday-Thursday 8am-6:30pm EST. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned (i.e., central fax phone number) is 571-273-8300.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Suresh Memula/

Art Unit 2825
February 3, 2010

/Phallaka Kik/
Primary Examiner, Art Unit 2825